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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/804,302	03/13/2001	Toru Otsuka	P 278088 T4A0-00S0902-1	9268

909 7590 07/16/2004

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EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/804,302	OTSUKA, TORU	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 069232.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/21/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 were examined.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy 2000-069232 was filed on 3/13/2000.

Information Disclosure Statement

3. The listing of references in the specification on page 1 is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A (1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." The examiner has acknowledged and accepts reference in the information disclosure statement. Furthermore, due to lack of English translation, the following references were not considered: 2707406 France; 19703090 Germany; 29709753 Germany; and 4407987 Germany.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure, which is not enabling. No detailed description of "third memory" in the specification.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

7. Regarding claim 11, the phrase "third memory" renders the claim indefinite because it is unclear whether the limitation following the phrase is part of the claimed invention. See MPEP § 2173.05(d).

8. Furthermore, claim 31 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The phrase "fist series" is undefined.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

10. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

11. Claims 1- 31 arte rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al., (U.S. Patent 6, 651,225 (1997)). Lin et al., teaches a verification dynamic logic evaluation system and method dynamically calculates the minimum evaluation time for each input (abstract).

Claim 1. A simulator is comprising: a simulation CPU (column 8, lines 53-65); a memory write-accessible from one of said simulation CPU and a control CPU connected to said simulator and read-accessible from the other (column 15, lines 5-10); means for causing said simulation CPU to read out control information written in said memory by the control CPU (column 15, lines 40-45); and means for writing an execution result of execution of simulation based on the control information in said memory in a state readable by the control CPU (column 15, lines 28-46).

Claim 2. A simulator according to claim 1, wherein said simulator further comprises connection means said simulation CPU to said memory, and for connecting the control

information is read out from said memory or the execution result is written in said memory through said connection means (column 15, lines 28-46).

Claim 3. A simulator according to claim wherein after the execution result of the simulation is written in said memory (column 15, lines 34-39), an interrupt is requested of the control CPU (column 112, lines 10-30).

Claim 4. A simulator according to claim 3, further comprising count means for counting the interrupt, and transmission means for transmitting timeout data on the basis of a count value of said count means (column 4, lines 29-39).

Claim 5. A simulator comprising (column 8, lines 53-65): a first memory in which control information is written by a control CPU connected to said simulator (column 15, lines 28-46; and column 119-120, lines 56-67 and 1-12, respectively); a second memory from which information can be read out by the control CPU (column 15, lines 40-45); means for reading out the control information from said first memory (column 15, lines 5-10; and column 120, lines 14-21); means for generating information of a control result based on the readout control information (column 48, lines 19-43); and means for writing the generated information of the control result in said second memory (column 23, lines 42-58).

Claim 6. A simulator according to claim 5(column 8, lines 53-65), wherein after the information of the control result is written in said second memory, an interrupt is requested of the control CPU (column 112, lines 10-30).

Claim 7. A simulator according to claim 6(column 8, lines 53-65; and column 112, lines 10-30) further comprising count means for counting the interrupt, and transmission means for transmitting timeout data on the basis of a count value of said count means (column 4, lines 29-39).

Claim 8. A simulator according to claim 5(column 8, lines 53-65) wherein the control information corresponds to a command, and the control result corresponds to a response (column 114, table H).

Claim 9. A simulator comprising: a first memory from which information can be read out by a control CPU connected to said simulator (column 15, lines 28-46; and column 119-120, lines 56-67 and 1-12, respectively); and means for periodically writing a sensor status in said first memory (column 168, claim 15 with column 15, lines 40-45).

Claim 10. A simulator according to claim 9(column 15, lines 28-46; and column 119-120, lines 56-67 and 1-12, respectively; and column 15, lines 40-45), further comprising a second memory in which command is written by the control CPU, means for reading out the command from said second memory (column 23, lines 42-58), means for

generating a response based on the readout command (column 114, table H), and means for writing the generated response in said first memory.

Claim 11. A simulator according to claim 10(column 15, lines 28-46; and column 119-120, lines 56-67 and 1-12, respectively; and column 15, lines 40-45), further comprising a third memory in which output port ON/OFF information is written by the control CPU, and means for reading out the output port ON/OFF information from said third memory (column 39, lines 39-54).

Claim 12. A simulator according to claim 9(column 15, lines 28-46; and column 119-120, lines 56-67 and 1-12, respectively), wherein in after first the sensor status is written memory, an interrupt is requested of the control CPU (column 112, lines 1-35).

Claim 13. A simulator according to claim 12(column 15, lines 28-46; and column 119-120, lines 56-67 and 1-12, respectively; and column 112, lines 1-35), further comprising count means for counting the interrupt, and transmission means for transmitting timeout data on the basis of a count value of said count means.

Claim 14. A method comprising the steps of: causing a control CPU to write control information in a first memory (column 8, lines 53-65); causing a simulation CPU to read out the control information written in the first memory; causing the simulation CPU to execute simulation based on the control information (column 15, lines 40-45); causing

the simulation CPU to write simulation result in a second memory (column 23, lines 42-58); and causing the control CPU result written in the second memory (column 112, lines 10-30).

Claim 15. A method according to claim 14(column 8, lines 53-65; column 15, lines 40-45; column 23, lines 42-58), further comprising the step of, after the simulation result is written in the second memory, requesting an interrupt of the control CPU (column 112, lines 1-35).

Claim 16. A method according to claim 15(column 8, lines 53-65; column 15, lines 40-45; column 23, lines 42-58), further comprising the steps of counting the interrupt, and transmitting timeout data on the basis of a count value of the interrupt (column 112, lines 1-35).

Claim 17. A simulator for simulating operation (column 8, lines 53-65) on a unit side in an apparatus which transmits command information from a main body side to the unit side transmits an execution result of the command from the unit side to the main body side as a response, and transmits sensor information on the unit side to the main body side, comprising (figure 45 with column 6, lines 42-44): a command memory for holding the command information transmitted from the main body side, said command memory being read-accessible from a unit-side CPU (figure 54, with column 6, lines 66-67); a sensor memory in which the sensor information can be written by the unit-side CPU

(column 168, claim 15); means for transmitting the sensor information written in said sensor memory to the main body side(column 168, claim 15); a response memory in which response information can be written by the unit-side CPU(column 168, claim 15); and means for transmitting the response information written in said response memory to the main body side(column 168, claim 15).

Claim 18. A simulator according to claim 17(column 8, lines 53-65; figure 45 with column 6, lines 42-44; column 168, claim 15), wherein said simulator further comprises an address memory for holding a self-address in advance and comparison means for comparing the self address held in said address memory with a designated address designated on the main body side, and by said comparison means indicates that the addresses match, the sensor information is received, the command information is received, and the response is sent (column 134, Table H).

Claim 19. A simulation system comprising (column 8, lines 53-65): a first simulator and a second simulator, each being connected to a main body, for simulating operation on a unit side, said first simulator comprising means for receiving sensor information transmitted from said second simulator to said main body side, and when a comparison result said first simulator operating in synchronism (column 151, lines 36-49) with said second simulator on the basis of the received sensor information.

Claim 20. A system according to claim 19(column 8, lines 53-65;column 151, lines 36-49), wherein said system simulates operation on a unit side using at least two simulators of an apparatus which transmits command information from the main body side to the unit side, transmits an execution result of the command from the unit side to the main body side as a response, and transmits sensor information on the unit side to the main body side, and said first simulator comprises a command memory for holding the command information transmitted from the main body side, said command memory being read-accessible from a unit-side CPU (column 167, claim 1 with column 134, Table H); a sensor memory in which the sensor information can be written by the unit-side CPU (column 168, claim 15); means for transmitting the sensor information written in said sensor memory to the main body side (column 167, claim 1 with figures 45 and 46); a response memory in which response information can be written by the unit-side CPU(column 167, claim 1); and means for transmitting the response information written in said response memory to the main body side(column 167, claim 1 with figures 45 and 46).

Claim 21. A system according to claim 20(column 167, claim 1 with figures 45 and 46), wherein said first simulator comprises a port memory for holding port information transmitted from the main body side, said port memory being read-accessible from the unit-side CPU (column 90 and 91, lines 36-67 and 1-51 respectively with figure 75).

Claim 22. A simulator for simulating operation on a command unit side information transmits an from a main body execution result of the command from the unit side to the main body side as a response transmits sensor information on the unit side to the main body side comprising(column 167, claim 1 with column 134, Table H): a first command memory for holding command said main body side via a information first accessible from transmitted from series, said first command memory being read-a unit-side CPU (column 90 and 91, lines 36-67 and 1-51 respectively with figure 75); a sensor memory in which the sensor information and which transmits in an apparatus side to the unit side, can be written by means for transmitting written in said sensor memory the unit-side CPU (column 4, lines 5-17) and ; the sensor information to said main body side via said first series(column 4, lines 5-17); a response memory in which response information can be written by the unit-side CPU (column 109, table F and lines 13-23); means for transmitting the response information written in said response memory to the main body side a second command memory for holding said main body command side via a being read-information transmitted from second series, said second command memory accessible from the unit-side CPU (column 109, lines 13 to column 110, lines 1-38).

Claim 23. A simulation system comprising: a first simulator and a second simulator said first simulator comprising means for receiving sensor information transmitted from said second simulator to said main body side via a second series, said first simulator operating in synchronism with said second simulator on the basis of the received sensor

information, said second simulator comprising means for receiving sensor information transmitted from said first simulator to said main body side via a first series, and said second simulator operating in synchronism with said first simulator on the basis of the received sensor information (column 4, lines 7-21 with column 109, lines 13 to column 110, lines 1-38).

Claim 24. A system according to claim 23(column 4, lines 7-21 with column 109, lines 13 to column 110, lines 1-38), wherein said system simulates operation on a unit side using at least two simulators of an apparatus which transmits command information from the main body side to the unit side, transmits an execution result of the command from the unit side to the main body side as a response and transmits sensor information on the unit side to the main body side, and said first simulator comprises a first command memory for holding command(column 90 and 91, lines 36-67 and 1-51 respectively with figure 75) information transmitted from said main body side via said first series, said first command memory being read-accessible from a unit-side CPU; a sensor memory in which the sensor information can be written by the unit-side CPU; means for transmitting the sensor information written in said sensor memory to said main body side via said first series (column 4, lines 5-17;and column 167, claim 1); a response memory in which response information can be written by the unit-side CPU (column 168, claim 15); means for transmitting the response written in said response memory to via said first series (column 167, claim 1); and a second command memory for holding command information transmitted from said second main body side via said

second series, said second command memory being read-accessible from the unit-side CPU (column 90 and 91, lines 36-67 and 1-51 respectively with figure 75).

Claim 25. A system according to claim 24(column 167, claim 1; and column 90 and 91, lines 36-67 and 1-51 respectively with figure 75), wherein said information said main body side first simulator comprises a port memory for holding port information transmitted from said main body side via said first series, said port memory being read-accessible from the unit-side CPU, and a port memory for holding port information transmitted from said main body side via said second series, said port memory being read-accessible from the unit-side CPU.

Claim 26. A simulation method of simulating operation on a unit side in an apparatus which transmits command information from a main body side to the unit side, transmits an execution result of the command from the unit side to the main body side as a response, and transmits sensor information on the unit side to the main body side, comprising the steps of (column 167, claim 1; column 134, Table H; and column 4, lines 5-18): holding the command information transmitted from the main body side a unit-side CPU (column 90 and 91, lines 36-67 and 1-51 respectively with figure 75); and transmitting sensor information and response information written by the unit-side CPU to the main body side (column 4, lines 5-18).

Claim 27. A simulation method system including first applied to a simulation and second simulators, comprising the steps of: causing the first simulator to receive sensor information transmitted from the second simulator to a main body side (column 167, claim 1; column 168, claim 16; and column 151, lines 36-65); and causing the first simulator to operate in synchronism with the second simulator on the basis of the received sensor information (column 167, claim 1; column 151, lines 36-65; and column 168, claim 16).

Claim 28. A method according to claim 27(column 167, claim 1; column 151, lines 36-65; and column 168, claim 16), wherein said method simulates operation on a unit side using at least two simulators of an apparatus which transmits command information from the main body side to the unit side, transmits an execution result of the command from the unit side to the main body side as a response, and transmits sensor information on the unit side to the main body side and said method further comprises the steps of causing the first simulator to hold the command information transmitted from the main body side in a state read-accessible from a unit-side CPU, and causing the first simulator to transmit the sensor information and response information written by the unit-side CPU to the main body side (column 4, lines 5-17; column 167, claim 1; and column 168, claim 15 with figure 45).

Claim 29. A simulation method of simulating operation on a unit side in an apparatus which transmits command information from a main body side to the unit side, transmits

an execution result of the command from the unit side to the main body side as a response, and transmits sensor information on the unit side to the main body side, comprising the steps of(column 4, lines 5-17; column 167, claim 1; and column 168, claim 15 with figure 45): holding command information transmitted from said main body side via a first series and command information transmitted from said main body side via a second series in a state read-accessible from a unit-side CPU (column 109, Table F and lines 13-65); and transmitting sensor information and response information written by the unit-side CPU to said main body side via said first series (column 4, lines 10-17; and column 109, Table F and lines 13-65).

Claim 30. A simulation method applied to a simulation system including first and second simulators and a main body comprising the steps of: causing the first simulator to receive sensor information transmitted from the second simulator to said main body side via a second series (column 4, lines 5-17; column 167, claim 1; and column 168, claim 15 with figure 45); causing the first simulator to operate in synchronism with the second simulator on the basis of the received sensor information (column 4, lines 7-21 with column 109, lines 13 to column 110, lines 1-38); causing the second simulator to receive sensor information transmitted from the first simulator to said main body side via a first series(column 4, lines 7-21 with column 109, lines 13 to column 110, lines 1-38); and causing the second simulator to operate in with the first simulator on the basis of synchronism the received sensor information (column 4, lines 7-21 with column 109, lines 13 to column 110, lines 1-38)

Claim 31. A method according to claim 30(column 4, lines 7-21 with column 109, lines 13 to column 110, lines 1-38), wherein said method simulates operation on a unit side using at least two simulators of an apparatus which transmits command information from the main body side to the unit side, transmits an execution result of the command from the unit side to the main body side as a response and transmits sensor information on the unit side to the main body side, and said method further comprises the steps of causing the first simulator to hold command information transmitted from said main body side via a first series and command information transmitted from said main body side via a second series in a state read-accessible from a unit-side CPU, and causing the first simulator to transmit the sensor information and response information written by the unit-side CPU to said main body side via a fist series (column 4, lines 5-17; column 167, claim 1; and column 168, claim 15 with figure 45).

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is (703) 305-0365, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Kevin Teska at (703) 305-9704. The fax number for the group is 703-872-9306.

Any inquires of general nature or relating to the status of this application should be directed to the Group receptionist whose phone number is (703) 305-3900.

July 7, 2004

THS

KEVIN J. TESKA
SUPERVISORY
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